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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,859	07/09/2003	Yasuo Inoue	29284/598	8149

7590 07/17/2006

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EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 07/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,859	INOUE, YASUO	
	Examiner	Art Unit	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/10/2006 has been entered.

Response to Arguments

2. Applicant's arguments and amendment to claims, filed 04/19/2006, with respect to the rejection(s) of claim(s) 1-18 under 35 U.S.C. §102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of US Pat. No. 5,325,488 to Carteau et al. (Carteau) cited in IDS submitted 09/27/2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 3-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Carteau.

5. Per Claim 1, Carteau discloses a storage system *(Fig. 1)* comprising: a channel unit *(Fig. 1, element HA1 or HA2 is the host adapter which is directly linked with the link channel, CE, hence, being the channel unit; Fig. 1 and Column 4, lines 25-35 disclose the Host, e.g., the upper level system, communicating with the storage system via the host adapter which controls/interfaces the link channel, CE)* that transfers data sent from an upper-level system *(Fig. 1, host are shown as H1, H2, etc)* and transfers data to said upper-level system *(Fig. 1, channels CE clearly shown as bidirectional)*, a cache unit which is coupled to said channel unit *(Fig. 1, CA1 is a cache unit)* and in which data sent from said channel unit is stored *(Fig. 8A shows HA1 writing a block to CA1)*; a plurality of control units that is coupled to said cache unit, and transfers or receives data to or from said cache unit *(Fig. 1, DA1 and DA2 are disk adaptors that control access to disk array BMD1 and the cache unit; Fig. 7B shows DA1 communicating with cache, CA1; Note, Carteau discloses a fully redundant system where if one unit fails, a corresponding duplicate unit performs the failed units duties, Column 5, lines 60-Column 6, lines 5; Thus DA1 and DA2 are clearly both coupled to CA1 via buses B1 and B2)*; a disk device that stores data written under control of each of said plurality of control units *(Fig. 1, elements D1-D6, all part of disk array BMD1)*; a plurality of paths *(Fig. 1, paths from each block via buses B1 and B2)*, a first one of said paths coupling said cache unit to a first one of said control units *(Fig. 1, path from CA1 to DA1 goes through bus B1)*, a second one of said paths coupling said cache unit to a second one

of said control units *(Fig. 1, path from CA1 to DA2 goes through bus B2)*; at least one first processor *(Fig. 3, element MPH1)* for controlling transfer to and from the cache unit of data which is transferred from said upper-level system and received at and transferred from said channel unit (*Column 6, lines 23-27, MPH1 is a microprocessor that controls functions of the channel unit HA1; Fig. 7A shows HA1 communicating with CA1*); and at least one second processor *(Fig. 3, element MPD1)* for controlling said cache unit to transfer data to said disk device *(Column 6, lines 55-60, MPD1 controls disk adapter DA1/DA2; Fig. 8A and 8B shows DA1/DA2 communicate with disk device and cache)*, wherein a number of said paths linking said plurality of control units and said cache unit are at least equal to a number of said plurality of control units *(Fig. 1, two disk adapters DA1 and DA2 have two distinct paths to the cache unit CA1 over buses B1 and B2)*.

6. Per Claims 3-10 and 12, Carteau discloses Claim 1, further disclosing two distinct paths on busses B1 and B2, one going from DA1 to CA1 and another going from DA2 to CA1 *(Fig. 1)* that do not overlap each other. Thus, each are dedicated, independent, direct, point-to-point and signal line type paths.

7. Per Claim 11, Carteau discloses Claim 1, further disclosing said disk device includes a plurality of disk drives *(Fig. 1, elements D1-D6)*, and plurality of control unit are connected to said plurality of disk drives *(Fig. 1, DA1 and DA2 are connected to disk drives through CS1 and CS3, respectively)*.

8. Per Claim 13, Carteau discloses Claim 1, Carteau further disclosing said plurality of paths are used to write data *(Figs. 8A and 8B show command of write to cache)*, of

which writing is requested by said upper-level system *(Fig. 8A, item 1 shows command to write by host to channel unit, HA1)*, from said cache unit to said disk device, and used to communicate data, of which writing is requested by said upper-level system, from said cache unit to said plurality of control units *(Fig. 8A, items 25+ shows communications between control unit (DA1 and MTD1), cache (CA1), disk drives (D1-D6))*.

9. Per Claim 14, Carteau discloses Claim 1, Carteau further disclosing said plurality of paths are used to read data *(Figs. 7A and 7B show command of read from cache)*, of which reading is requested by said upper-level system *(Fig. 7A, item 1)*, from said disk device, and are used to communicate data, of which reading is requested by said upper-level system, from said control unit to said cache unit *(Fig. 7A, items 4+ show communications between control unit, cache and disk drives)*.

10. Per Claims 15-18, Carteau discloses Claim 1, Carteau further disclosing MPH1 and MPD1 as the two microprocessors *(Fig. 3)* that control functions of the channel unit *(HA1)* and control unit *(DA1)*, respectively *(Column 6, lines 23-27 and 55-60)*. Figures 7 and 8 of Carteau shows communications of both channel unit and control unit with the cache unit *(CA1)* and disk drives *(D1-D6)*, the processing of the communications ultimately performed by the two microprocessors.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Alan S. Chen

7/8/06

ASC
07/08/2006